APPENDIX

AMENDED CLAIMS SHOWING AMENDMENTS

3. (amended) A digital processing system comprising:

processing circuitry;

a system memory coupled to said processing circuitry; and

[a programmable logic device as defined in claim 1] coupled to the processing circuitry and the system memory, a programmable logic device comprising:

a plurality of logic resources,

a plurality of groups of interconnection conductors for interconnecting said logic resources, and

a plurality of programmable interconnection resources for connecting conductors in said groups of interconnection conductors to one another and to said plurality of logic resources, said programmable interconnection resources being less than fully populated, said programmable logic device further comprising:

at least one random access memory having a read port and a write port,

a first programmable interconnection resource in said plurality of programmable interconnection resources for connecting port conductors in said read port to a selected one of said plurality of groups of interconnection conductors, and

a second programmable interconnection resource in said plurality of programmable interconnection resources for connecting port conductors in said write port to said selected one of said plurality of groups of interconnection conductors, wherein:

said first and second programmable interconnection resources are populated to allow connection of an individual conductor in said selected one of said plurality of groups of interconnection conductors to

corresponding port conductors in both said read port and said write port.

4. (amended) A printed circuit board on which is mounted a programmable logic device [as defined in claim 1], said programmable logic device comprising:

a plurality of logic resources;

a plurality of groups of interconnection conductors for interconnecting said logic resources; and

a plurality of programmable interconnection resources for connecting conductors in said groups of interconnection conductors to one another and to said plurality of logic resources, said programmable interconnection resources being less than fully populated; said programmable logic device further comprising:

at least one random access memory having a read port and a write port;

a first programmable interconnection resource in said plurality of programmable interconnection resources for connecting port conductors in said read port to a selected one of said plurality of groups of interconnection conductors; and

a second programmable interconnection resource in said plurality of programmable interconnection resources for connecting port conductors in said write port to said selected one of said plurality of groups of interconnection conductors; wherein:

said first and second programmable interconnection resources are populated to allow connection of an individual conductor in said selected one of said plurality of groups of interconnection conductors to corresponding port conductors in both said read port and said write port.

9. (amended) A digital processing system comprising:

processing circuitry;

a system memory coupled to said processing circuitry; and

[an integrated circuit as defined in claim 7] coupled to the processing circuitry and the system memory, an integrated circuit comprising:

a plurality of semiconductor devices,

a plurality of groups of interconnection conductors for interconnecting said semiconductor devices, and

a plurality of programmable interconnection resources for connecting conductors in said groups of interconnection conductors to one another and to said plurality of semiconductor devices, said programmable interconnection resources being less than fully populated, said integrated circuit further comprising:

at least one random access memory having a read port and a write port,

a first programmable interconnection resource in said plurality of programmable interconnection resources for connecting port conductors in said read port to conductors in a selected one of said plurality of groups of interconnection conductors, and

a second programmable interconnection resource in said plurality of programmable interconnection resources for connecting port conductors in said write port to conductors in said selected one of said plurality of groups of interconnection conductors, wherein:

said first and second programmable interconnection resources are populated to allow connection of an individual conductor in said selected one of said plurality of groups of interconnection conductors to corresponding port conductors in both said read port and said write port.

10. (amended) A printed circuit board on which is mounted [a programmable logic device as defined in claim 7] an integrated circuit, said integrated circuit comprising:

a plurality of semiconductor devices;

a plurality of groups of interconnection conductors for interconnecting said semiconductor devices; and

a plurality of programmable interconnection resources for connecting conductors in said groups of interconnection conductors to one another and to said plurality of semiconductor devices, said programmable interconnection resources being less than fully populated; said integrated circuit further comprising:

at least one random access memory having a read port and a write port;

a first programmable interconnection resource in said plurality of programmable interconnection resources for connecting port conductors in said read port to conductors in a selected one of said plurality of groups of interconnection conductors; and

a second programmable interconnection resource in said plurality of programmable interconnection resources for connecting port conductors in said write port to conductors in said selected one of said plurality of groups of interconnection conductors; wherein:

said first and second programmable interconnection resources are populated to allow connection of an individual conductor in said selected one of said plurality of groups of interconnection conductors to corresponding port conductors in both said read port and said write port.